Notice of Allowability	Application No.	Applicant(s)	
	10/705,317	MATHEW ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 10/11/05*.

2. ☒ The allowed claim(s) is/are *1-12,14-28 and 30-39*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Robert King on January 20, 2006.

The application has been amended as follows:

Claims:

Cancel claim 13

1. (Currently Amended) A method of making a semiconductor device comprising:
forming a semiconductor channel structure, the semiconductor channel structure including a top horizontal surface, a first vertical sidewall, and a second vertical sidewall opposing the first sidewall;
forming a first gate structure and a second gate structure, wherein the first gate structure is located laterally adjacent to and substantially along the first sidewall and the second gate structure is located laterally adjacent to and substantially along the second sidewall; ~~and~~
forming a third gate structure located over and substantially along all of the top horizontal surface, wherein the first gate structure, the second gate structure, and the third gate structures are physically separate from each other,

wherein forming the first gate structure and the second gate structure further comprises depositing a layer of gate material over both the third gate structure and a substrate, and removing a portion of the layer of gate material overlying the third gate structure to form the first gate structure and the second gate structure**; and**

forming a charge storage layer between the semiconductor channel structure and at least one gate structure selected from a group consisting of the first gate structure, the second gate structure and the third gate structure.

5. (Currently Amended) A method of making a semiconductor device comprising:

forming a semiconductor channel structure, wherein the semiconductor channel structure is formed from a layer of semiconductor material, the semiconductor channel structure including a top surface, a first sidewall, and a second sidewall opposing the first sidewall;

forming a first gate structure and a second gate structure, wherein the first gate structure is located laterally adjacent to and substantially along the first sidewall and the second gate structure is located laterally adjacent to and substantially along the second sidewall; ~~and~~

forming a third gate structure located over and substantially along all of the top surface, wherein the first gate structure, the second gate structure, and the third gate structures are physically separate from each other,

wherein forming the third gate structure includes forming a layer of gate material over the semiconductor material and patterning the layer of gate material and layer of semiconductor material with a single patterning step**; and**

forming a charge storage layer between the semiconductor channel structure and at least one gate structure selected from a group consisting of the first gate structure, the second gate structure and the third gate structure.

Allowable Subject Matter

Claims 1-12,14-28 and 30-39 are allowed.

The following is an examiner's statement of reasons for allowance: Claims 1-12 and 14-24 are allowable because prior art does not disclose alone or in combination along with the limitations of the independent claims such as forming a charge storage layer between the semiconductor channel structure and at least one gate structure selected from a group consisting of the first gate structure, the second gate structure and the third gate structure.

The following is an examiner's statement of reasons for allowance: Claims 25-28 and 30-38 are allowable because prior art does not show alone or in combination along with the limitations of the independent claim such as a first charge storage structure located between the top surface and the third gate structure.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

Zandra V. Smith
Supervisory Patent Examiner
23 Jan 2006